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Daffodil International University

Faculty of Science & Information Technology
Department of Software Engineering
Final Examination, Fall 2024
Course Code: SE222 ; Course Title: Computer Architecture
Sections & Teachers: All

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	*a)*	**Explain** the three key performance parameters of memory systems with appropriate equation.	[Marks-5]	CLO-2 *Level-2*
	b)	**Describe** the structure of cache memory and Explain the process of a cache read operation with proper diagram.	[Marks-5]	
2.	*a)*	**Demonstrate** your understanding of cache mapping techniques by explaining how each method resolves cache conflicts theoretically.	[Marks-7]	CLO-3 *Level-3*
	b)	**Apply** the Booth's algorithm for 2's complement multiplication for the following values: (Using 4 bits) **Multiplier: -5** **Multiplicand: -7**	[Marks-5]	
	c)	**Calculate** the following floating point binary numbers into denary. Assuming 10 bits for the mantissa and 6 bits for the exponent, both in 2's complement. 0 1 0 0 0 0 1 0 0 0 1 1 1 1 0 1 1 0 1 1 1 1 0 1 1 0 1 1 1 1 1 0	[Marks-8]	
3.	*a)*	**Investigate** the following expression, representing it as coding for both two-address and one-address representations: $Z = [\{(b * b) + (c * c)\} - (ab + bc + ca)]$	[Marks-5]	CLO-4 *Level-3*
	b)	**Model** the pipeline architecture for an instruction set with 21 instructions, following the considerations - 2nd instruction is a branch instruction which indicates 12th instruction. 12th instruction is another branch instruction which indicates 19th instruction.	[Marks-5]	