



Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Midterm Examination, Fall 2025
Course Code: SE 222; Course Title: Computer Architecture
Sections & Teachers: A to O (SR, FBR, AS, HKN)

Time: 1 Hour 30 Mins

Marks: 25

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	A processor has base clock speed of 500 MHz. It is used to execute a benchmark program with the following instruction mix and clock cycle count. <table><tr><th>Instruction Type</th><th>CPI</th><th>No of instructions</th></tr><tr><td>Arithmetic</td><td>2</td><td>7000</td></tr><tr><td>Floating Point</td><td>3</td><td>5000</td></tr><tr><td>Data Transfer</td><td>4</td><td>3000</td></tr><tr><td>Control Transfer</td><td>5</td><td>2000</td></tr></table> Compute the effective CPI and Execution Time for this program.	Instruction Type	CPI	No of instructions	Arithmetic	2	7000	Floating Point	3	5000	Data Transfer	4	3000	Control Transfer	5	2000	[Marks-4]	CLO-1 Level-2																					
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Control Transfer	5	2000																																						
	b)	For Question 1(a) Option 1: Reduce CPI of Floating point type to 1.5 Option 2: Reduce CPI of data transfer type to 2 Estimate the better option in terms of MIPS rate.	[Marks-4]																																					
	c)	Clarify the top level components of GP processor along with diagram.	[Marks-4]																																					
	d)	Suppose a program runs in 60 seconds on a machine with the instruction of A and B. Instruction A type is for 45 seconds of this time. Compute the improvement (%) of A type instruction if we want the program to run 3 times faster?	[Marks-3]																																					
2.	a)	<table><tr><th colspan="2">Memory</th><th colspan="2">CPU Register</th></tr><tr><td>300</td><td>1941</td><td>300</td><td>PC</td></tr><tr><td>301</td><td>C942</td><td></td><td>AC</td></tr><tr><td>302</td><td>2942</td><td></td><td>IR</td></tr><tr><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td></tr><tr><td>941</td><td>0004</td><td></td><td></td></tr><tr><td>942</td><td>0002</td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td></tr></table> Where A=10, B=11, C=12, D=13, E=14, F=15 Explain the execution steps of Hypothetical Processor for the given scenario. Here memory contents are represented in hexadecimal 0001---Load AC from Memory 1100---Subtract AC from Memory 0010---Store AC to Memory Location	Memory		CPU Register		300	1941	300	PC	301	C942		AC	302	2942		IR									941	0004			942	0002							[Marks-4.5]	CLO-2 Level-4
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	b)	Compare Instruction cycle without and with interrupt.	[Marks-2.5]																																					
	c)	Differentiate Register, Cache, and Main Memory based on their Performance, roles and working principles.	[Marks-3]																																					