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Daffodil International University

Department of Software Engineering

Faculty of Science & Information Technology

Final Examination, Fall 2023

Course Code: SE 213; Course Title: Digital Electronics & Logic design

Batch: 40; Sections: All

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1	a)	Apply k-map simplification technique to simplify the following function. Construct the logic diagrams of the simplified output. $F(m,n,o,p) = \sum (0,2,4,5,6,7,12,13,14,15)$	[Marks-5]	CLO-2 *Level-3*
	b)	Design a full adder by obtaining the simplified expressions for the sum And carry outputs using basic logic gates.	[Marks-5]	
2	a)	Develop 4 to 16 decoder using 3 to 8 decoder.	[Marks-5]	CLO-3 *Level-3*
	b)	Utilize the concept of an Encoder circuit to build Octal to binary converter.	[Marks-5]	
	c)	Build the following function using Multiplexer. $F(A,B,C,D) = \sum (1,2,4,7,10,12,13,14,15)$	[Marks-5]	
	d)	Design an 8X1 Demultiplexer following necessary steps.	[Marks-5]	
3	a)	Explain the working principle of Serial Input serial Output (SISO) Shift register.	[Marks-5]	CLO-4 *Level-5*
	b)	"JK flip flop is used to remove the drawback of the S-R flip flop". Justify the above statement with appropriate circuit diagram.	[Marks-5]	