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Quiz Test 03 (Set A)

Student ID: _____ Student Name: _____

Course Code: CIS131 **Course Title: Computer Architecture and Organization**
Semester: Summer 2026 **Section: 24C** **Date: 30.07.2026**
Exam Duration: **20 mins** Marks: **15**

1. **Which register holds operands and results of ALU operations?**
   - ☐ IR
   - ☐ ACC
   - ☐ MAR
   - ☐ PC

2. **During which phase are MemRead, IRWrite, and PCWrite typically active?**
   - ☐ Store
   - ☐ Execute
   - ☐ Decode
   - ☐ Fetch

3. **What does "AMAT" stand for?**
   - ☐ Average Memory Allocation Time
   - ☐ Average Memory Access Time
   - ☐ Average Miss Access Time
   - ☐ Average Memory Access Table

4. **In a 1000-reference example, if L1 misses 40 times, what is the L1 Local Hit Rate?**
   - ☐ 96%
   - ☐ 2%
   - ☐ 40%
   - ☐ 4%

5. **What are the two types of logic elements in a datapath?**
   - ☐ Static and Dynamic
   - ☐ Serial and Parallel
   - ☐ Combinational and State
   - ☐ Volatile and Non-volatile

6. **The datapath and control unit together form what?**
   - ☐ Compiler
   - ☐ Memory
   - ☐ Operating System
   - ☐ Processor

7. **In direct-mapped cache placement, a block's location is determined by:**
   - ☐ Memory Block number MOD number of sets in a cache
   - ☐ Memory Block number MOD number of cache blocks
   - ☐ Random assignment
   - ☐ Only in L1 cache

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8. **What is the first step in the Fetch phase?**

☐ MAR ← PC ☐ IR ← MDR ☐ PC ← PC+1 ☐ MDR ← Memory[MAR]

9. **What technology is typically used for L1/L2/L3 cache?**

☐ DRAM ☐ SRAM ☐ Flash memory ☐ Magnetic disk

10. **What does "temporal locality" refer to?**

☐ Accessing nearby memory addresses
☐ Accessing data sequentially
☐ Reusing recently accessed data/instructions
☐ Accessing data from disk

11. **Which write policy updates both the cache and lower-level memory simultaneously on a write hit?**

☐ Write-Back ☐ Write-Through
☐ Write-Allocate ☐ No-Write Allocate

12. **Which replacement policy evicts the block that has not been used for the longest time?**

☐ FIFO ☐ Random ☐ Round Robin ☐ LRU

13. **Which level of the memory hierarchy sits closest to the processor?**

☐ CPU Registers ☐ L1 Cache ☐ Main Memory ☐ Hard Disk

14. **Which is an advantage of Hardwired Control Units?**

☐ Easy to modify after fabrication
☐ Very fast, pure hardware, no lookup delay
☐ Best suited for CISC ISAs
☐ Requires control store

15. **In Immediate addressing mode, where is the operand found?**

☐ Memory ☐ Register ☐ In the instruction itself
☐ At an address stored in another register

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Quiz Test 03 (Set B)

Student ID: _____ Student Name: _____

Course Code: CIS131
Semester: Summer 2026
Exam Duration: **20 mins**

Course Title: Computer Architecture and Organization
Section: 24C

Date: 30.07.2026
Marks: **15**

1. **What is the role of the MAR?**
   - ☐ Holds the data fetched from memory
   - ☐ Holds the address to read/write from memory
   - ☐ Holds the current instruction
   - ☐ Holds ALU operation results

2. **Which control signal triggers memory to output data?**
   - ☐ MemWrite
   - ☐ IRWrite
   - ☐ RegWrite
   - ☐ MemRead

3. **In direct-mapped cache placement, a block's location is determined by:**
   - ☐ Memory Block number MOD number of sets in a cache
   - ☐ Memory Block number MOD number of cache blocks
   - ☐ Random assignment
   - ☐ Only in L1 cache

4. **Which is the correct order of the single-cycle design stages?**
   - ☐ Instruction Decode, Instruction Fetch, Execute, Register Fetch, Memory Access, Write Back
   - ☐ Instruction Fetch, Instruction Decode, Register Fetch, Execute, Memory Access, Write Back
   - ☐ Instruction Fetch, Instruction Decode, Memory Access, Register Fetch, Execute, Write Back
   - ☐ Register Fetch, Instruction Fetch, Instruction Decode, Execute, Write Back, Memory Access

5. **The datapath and control unit together form what?**
   - ☐ Compiler
   - ☐ Memory
   - ☐ Operating System
   - ☐ Processor

6. **In a 1000-reference example, if L1 misses 40 times, what is the L1 Local Miss Rate?**
   - ☐ 96%
   - ☐ 2%
   - ☐ 40%
   - ☐ 4%

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7. **Which level of the memory hierarchy sits closest to the processor?**
   ☐ CPU Registers ☐ L1 Cache ☐ Main Memory ☐ Hard Disk

8. **In the Fetch phase, which register change occurs last?**
   ☐ MAR ← PC ☐ MDR ← Memory[MAR] ☐ IR ← MDR ☐ PC ← PC + 1

9. **What technology is typically used for L1/L2/L3 cache?**
   ☐ DRAM ☐ SRAM ☐ Flash memory ☐ Magnetic disk

10. **What does "AMAT" stand for?**
    ☐ Average Memory Allocation Time
    ☐ Average Memory Access Time
    ☐ Average Miss Access Time
    ☐ Average Memory Access Table

11. **What does "spatial locality" refer to?**
    ☐ Accessing items whose addresses are close together
    ☐ Reuse of the same data over time
    ☐ Accessing random memory locations
    ☐ Accessing registers only

12. **In Immediate addressing mode, where is the operand found?**
    ☐ Memory ☐ Register ☐ In the instruction itself
    ☐ At an address stored in another register

13. **Which write policy on a write miss allocates a cache block before writing, and is typically paired with write-back caches?**
    ☐ No-Write Allocate ☐ Write-Through
    ☐ Write Allocate ☐ Write-back

14. **Which replacement policy evicts the block that has not been used for the longest time?**
    ☐ FIFO ☐ Random ☐ Round Robin ☐ LRU

15. **Which is an advantage of Hardwired Control Units?**
    ☐ Easy to modify after fabrication
    ☐ Very fast, pure hardware, no lookup delay
    ☐ Best suited for CISC ISAs
    ☐ Requires control store