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Daffodil International University

Faculty of Science & Information Technology

Final Examination, Spring 2023

Course Code: CSE411 Course Title: Computer Architecture and Organization

Level:4 Term:1 Batch:55

Time: 2 Hours **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	Suppose, you are a software engineer working on a large-scale application that processes and analyzes massive amounts of data. The application is running on a server with limited physical memory, and you are tasked with optimizing its performance. Now, analyzing the above scenario, which approach will you use for this scenario? How does it differ from physical memory?	[5]	CO3
	b)	Also discover the potential challenges or drawbacks might arise when implementing your approach for the above scenario? And how would you determine the size and tracking for processing the large-scale application?	[5]	
	c)	"Complicated arithmetic operations like exponentiation and trigonometric functions are costly to implement in CPU hardware, while software implementations of these operations are slow." Identify the solution to this problem.	[2]	
2.	a)	Instruction pipeline is a technique used in modern processors to improve their performance. The main advantage of an instruction pipeline is that it can increase the overall throughput of the processor. Now, sketch the flowchart of six stage instruction pipeline.	[3]	CO1
	b)	Illustrate the basic structure of a pipeline with 4 segments or stages considering a single register or latch R, and a single datapath circuit C_i constitutes a stage.	[2]	
3.	a)	Suppose, processor need to execute the following instructions: *Instruction1*: $R \leftarrow P + Q$ *Instruction2*: $S \leftarrow T + R$ *Instruction3*: $S \leftarrow W + M$ *Instruction4*: $W \leftarrow G - H$ *Instruction5*: $H \leftarrow W + 1$ *Instruction6*: $W \leftarrow 2 + S$	[6+3]	CO4

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		Now, analysing the given sequential instructions, draw two different timing diagrams (one for normal manner with data hazard and another one with the solution to prevent data hazard) using 6 stage instructions pipeline. Also identify with proper explanation that how many hazards could happen in the given scenario and how could you solve those.		
	b)	Demonstrate the multiplication of fixed-point numbers 1010 and 1100 using repeated shifts and add operations. Also, depict the 4x4 AND array circuit needed for implementing it in the hardware.	[4]	
4.	*a)*	John is playing his favorite video game on his computer, and he notices that the game is running slow. He decides to upgrade his computer's memory to improve its performance. After some research, he learns about cache memory, which is faster than regular memory and can be used to store frequently accessed data. He also observes that one cache mapping is faster for searching and one is comparatively slow as it uses multi-level cache in cache mapping. Now, analyzing the above scenario, illustrate the process of those two-cache mapping with the help of mapping diagram and addressing structure.	[8]	CO2
	b)	Demonstrate the process of cache read operation using a flow chart.	[2]	