ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

Daffodil International University

Faculty of Science & Information Technology
Department of Computing and Information System
Final Examination, Summer-2026
Course Code: CIS131, Course Title: Computer Architecture and Organization
Level: 1 Term: 2

Exam Duration: 2 Hours **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	***a)***	ArcticSense Ltd. builds a low-cost weather-logging device that stores each temperature reading in a 32 bit floating-point register, where the exponent is represented in excess-64 (biased) form. During a cold-snap test, the sensor records $-(472.25)_{10}$°C. Determine the 32-bit representation of this value using an explicit mantissa representation.	**[4]**	**CO1**
	b)	While reviewing ArcticSense's ALU design, a new hardware engineer asks why the team chose 2's complement instead of sign-magnitude for representing signed integers. Justify why computers use 2's complement in representing signed integers.	**[2]**	
	c)	A startup is choosing a processor design philosophy for its new smartphone chip. One engineer argues for a RISC-based design, while another insists CISC would need fewer instructions per program. Explain the differences between RISC and CISC architectures to help resolve the debate.	**[3]**	
	d)	A compiler engineer is generating code for a stack-based virtual machine that only supports a Stack ISA (no registers). Show how the expression **A = (B * D) – (C + D * F)** would be evaluated on this machine using a Stack ISA.	**[3]**	
2.	***a)***	A video streaming server spends part of its time on video encoding and the rest on network I/O and other tasks. To cut costs, the operations team upgrades to a new GPU-based encoder that makes the encoding process 4 times faster, while everything else remains unchanged. If encoding accounts for 15% of the total execution time, find the overall system speedup achieved by upgrading to the GPU encoder, and express this speedup as a percentage speed increase.	**[3]**	**CO2**
	b)	TechCorp's R&D team is benchmarking two candidate server processors, P1 and P2, before choosing one for their next data-centre rollout. Program A is profiled on P1 (5.6 GHz): it has 9000 instructions, of which 25% are branch, 40% are load/store, and 35% are ALU instructions. Program D is profiled on P2 (6.2 GHz): it has 10,500 instructions, of which 20% are branch, 50% are ALU, and the rest are load/store instructions. On both processors, branch instructions have an average CPI of 3 and ALU instructions have	**[4]**	

ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

		an average CPI of 2, but load/store CPI differs 2 on P1 and 3 on P2. I. Find the clock cycle time (CCT) for each processor. II. Calculate the average CPI for both. III. Calculate the execution time for both. IV. Determine which processor is faster and by what speedup factor.		
	c)	A computer-architecture student is testing a simple CPU simulator and needs to verify it step by step before submitting a lab report. For the instruction LOAD R2, (300) "LOAD the value in R2 into memory address 300" assume the Program Counter (PC) currently holds address 150 and register R2 contains the value 42. Provide a full instruction cycle trace, showing the Phase, Action, and Register State at each step of the cycle (Fetch, Decode, Evaluate Address, Fetch Operand, Execute, Store).	[7]	
3.	*a)*	A gaming-laptop manufacturer's marketing team wants to understand why their new model "feels faster" despite using the same CPU clock speed as last year's model, and the answer lies in the redesigned memory hierarchy. What is Memory hierarchy, and how does it improve system performance?	[3]	CO3
	b)	A performance engineer is profiling a web server's cache subsystem. Over a monitoring window, the CPU generates 2,000 memory references: all 2,000 go to the L1 Cache; the L1 cache misses 100 times (1,900 hits at L1); those 100 misses are forwarded to the L2 Cache; out of those 100 accesses, the L2 cache misses 25 times; the remaining 25 misses are resolved by Main Memory. I. Find the Local Hit Rate and Local Miss Rate for L1 and L2. II. Find the Global Hit Rate and Global Miss Rate for L1 and L2.	[2+2]	
4.		An embedded-systems team is designing the memory-management unit for a 32-bit device with 1MB of RAM and a page size of 256 bytes. Before finalizing the design, the lead engineer asks the junior developer to work out the addressing scheme. I. What are the three fundamental problems that arise when directly accessing physical memory, and how can these issues be resolved? II. Determine the number of bits in the Virtual Address and how many bits are used for the Virtual Page Number, Physical Page Number, and the Page Offset.	[4+3]	CO3