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Daffodil International University

Faculty of Science & Information Technology

Department of Software Engineering

Midterm Examination, Fall_2026

Course Code: SE 213; Course Title: Digital Electronics & Logic design

Sections & Teachers: SP, MTE, RHA, SPB ,Batch and Section:47 (A-H)

Time: 1:30 Hrs **Marks: 25**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1	*a)*	**Convert** the following numbers: $(9AF3.31A)_{16} + (1011101.1101)_2 = (?)_{10}$	[Marks-3]	CLO-1 *Level-2*
	b)	**Subtract** binary number the following using 2's complement: i) $(31)_{10} - (63)_{10}$	[Marks-2]	
	c)	A robotic welding cell is controlled by a small digital circuit. The circuit reads three sensors and drives the welding torch and a warning light. Inputs: A = 1 if the safety door is closed; B = 1 if the operator is inside the work zone; C = 1 if the workpiece is clamped. Outputs: W (welding torch ON), L (warning light ON). (1) The torch stays OFF if the workpiece is not clamped, or if the operator is inside the work zone while the door is closed, or if the operator is inside the work zone while the door is open. In every other situation, the torch turns ON. (2) The warning light turns ON if the workpiece is not clamped and the door status and the operator's position are "in agreement" (the door is closed and the operator is inside, or the door is open and the operator is	[Marks- 5]	

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		outside). The light also turns ON if the workpiece is clamped, the door is closed and the operator is inside. **Express** the Boolean expression for each output, and then: i) Simplify each expression. ii) Draw the circuit diagram of the simplified expressions using AND, OR and NOT gates as required.		
2	*a)*	ii) Apply Parallel full adder to **Compute** (H + I) the following operation along with diagram: Where H = 1 1 0 0 1 1 and I = 1 1 0 0	[Marks-4]	CLO-2 *Level-3*
	b)	i) **F (Q, R, S) = ∑ (0, 1, 2, 4, 5, 6)** Apply k-map simplification technique to simplify the above expressions. **Construct** the logic diagrams of the simplified output.	[Marks-3]	
	c)	F (A, B, C, D) = C'(A'BD'+D') +AB'C+BD' Apply k-map simplification technique to simplify the above expressions. **Construct** the logic diagrams of the simplified output.	[Marks-8]	