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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Final Examination, Summer 2025
Course Code: CSE413 Course Title: Computer Architecture and Organization
Level:3 Term:1 Batch:64

Time: 2:00 Hrs **Marks: 40**

Answer ALL the Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes]

1.	a)	A computer engineering student is working on designing a custom embedded processor for a robotics project. While testing mathematical operations for sensor data processing, she realizes that complex operations are significantly slowing down the main processor. What could be a suitable solution to offload complex operations from the main processor by **explaining the concept** and working principle of that solution.	[3]	CO2
	b)	Using the long division (paper-pencil) method, divide the binary number 1110_2 by 10_2. **Show** the division process clearly, including subtraction steps at each stage. Provide the final products: **Quotient** and **Remainder**.	[3]	
2.	a)	From the below instructions **identify** what kind of data hazards are happening there in the timing diagram of five stages (FI, DI, FO, EI, WO). Justify your answer by performing all the instructions together on **a single timing diagram**. Finally **show one solution** timing diagram to **avoid** the particular hazards that occurred. Initially assume, \$T0 = 5, \$T1 = 10 **I1**: ADD \$T2, \$T0, \$T1 *// T2 = T0 + T1* RAW **I2**: MUL \$T3, \$T2, 2 **I3**: ADD \$T4, \$T0, \$T3 RAW **I4**: SUB \$T1, \$T4, \$T2 *// T1 = T4 – T2* **I5**: MUL \$T2, \$T0, \$T1	[3+4]	CO3
	b)	A student is analyzing the behavior of a **5-stage instruction pipeline** in a modern processor. The program being executed consists of **15 instructions.** The pipeline encounters **two conditional branches**: • **First Branch:** After **Instruction-4**, where **Instruction-12** should execute only if the branch is taken. • **Second Branch:** After **Instruction-12**, where **Instruction-6** should execute only if this branch is taken. **Illustrate** the effect of both branches on the pipeline operation using a single **timing diagram** and **discuss** the impact on instruction flow	[5]	

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3.	*a)*	A computing device is being designed to handle large-scale data processing efficiently. This system uses a **cache** of size **32,768 bits** and a **RAM** of size **32 KB** and a **block size** of **64 bytes**, and each byte needs a unique address for address translation. At the initial design phase, a **direct mapped** cache is used. **Sketch** the Cache and RAM structure with calculated blocks for the above requirements. **Show** the direct mapping diagram on that same structure using the law (k mod n) where k represents corresponding block number in RAM and n represents total number of lines in cache with address translation.	[4+3]	CO4
	b)	i. **Find** out the percentage of data loss possibility of cache memory in detail for the above structure with direct mapping. ii. **How** you will reduce the data loss to **75%** for the above scenario by updating the size of the single cache.	[4+3]	
4.	*a)*	You are playing a **128 GB** open-world game, on your computer that has only 8 GB of RAM. Along with the game, a Chrome tab is open for a walkthrough guide, and two PDFs are running in the background. Still, your system performs without crashing or freezing. ***Identify*** *the* **memory** management technique and type of memory that supports *this and* ***illustrate*** **how** the system can run such a high-memory-demanding game with limited physical RAM with diagram.	[4]	
	b)	Assume a specific game map section is not found in that special memory when requested during gameplay. **Describe** what the operating system does when a required portion of the game data is not present in that memory.	[4]	

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