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Daffodil International University

Department of Electrical and Electronic Engineering
Faculty of Engineering
Final Examination, Summer-2026

Course Code: 0714-323 | Course Title: Digital Electronics
Section: A, B, C, D, E | Level-Term: L3-T1 | Teacher's Initial: DAS, BS
Full Marks: 40 | Exam Date: August 22 , 2026 | Time: 2 Hours

[Notes: Answer all the questions. The number on the rightmost side of the question indicates the marks]

Q1. (a) **Derive** the truth table and, hence, **draw** the corresponding logic diagram for a BCD-to-decimal decoder. CO3 (C3) **6+5**

(b) **Implement** the Boolean function, $F(A, B, C, D) = \sum(0, 1, 3, 5, 13)$ using a multiplexer. Use A, B, and D as the selection lines of the multiplexer.

Q2. (a) **Implement** the following Boolean functions using PLA CO3 (C3) **5+3**
$F_1 = A'B'C' + A'BC + AB'C' + ABC$ and $F_2 = A'B'C + A'BC' + AB'C + ABC$

(b) JK flip flop is called the refinement of SR flip flop- **Justify** the statement with a suitable explanation. (C4)

Q3. Consider a synchronous sequential circuit consisting of two JK flip-flops, A and B, with a single input x. The input equations of the flip-flops are given below: CO3 (C4) **10**
$J_A = x, K_A = B', J_B = x$ and $K_B = A$

i) **Draw** the complete logic diagram of the sequential circuit.

ii) **Derive** the state equations, **construct** the state table and **draw** the corresponding state diagram of the circuit.

Q4. (a) **Design** a synchronous counter using T flip-flops that follows the counting sequence: CO3 (C3) **7+4**
0, 1, 3, 4, 5, 7 and repeat.

(b) **Draw** and **explain** the operation of a 3-bit right-shift register using D flip-flops.



