ourdiu.com | Shared by Abid Hossan Farhan

Daffodil International University

Faculty of Science & Information Technology
Department of Computing and Information System
Final Examination, Spring-2026
Course Code: CIS131, Course Title: Computer Architecture and Organization
Level: 1 Term: 2

Exam Duration: 2 Hours **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	**(a)**	Define Instruction Set Architecture (ISA) and explain its role in computer systems.	[2]	**CO1**
	(b)	Convert $(-516.80)_{10}$ in IEEE-754 32-bit floating point number with your final answer represented in hexadecimal.	[4]	
	(c)	A program executes 1,000,000 instructions with CPI = 2 and Clock rate = 2 GHz i) Calculate the execution time. ii) Explain how does performance change if CPI is reduced to 1.5?	[4]	

2.	**(a)**	Which mapping technique reduces conflict misses? Analyze the reasons behind its effectiveness compared to other mapping techniques.	[3]	**CO2**
	(b)	During the recent "MVP Competition for AI-Driven Departments at DIU", student teams proposed various AI solutions such as smart evaluation systems and real-time decision-making tools. One team developed an AI-based evaluation system that processes student scores using arithmetic operations and immediate values (e.g., adding bonus marks or adjusting thresholds). To efficiently support such operations, the processor must execute R-type and immediate-type instructions. Based on this scenario, answer the following questions: (i) The system executes the following instruction to update a student's score: ADD R1, R2, R3 where R2 & R3 contain input scores, and R1 stores the computed result. Now, Illustrate and explain the single-cycle datapath required to execute this R-type instruction.	[6+6]	

ourdiu.com | Shared by Abid Hossan Farhan

		(ii) To apply bonus marks, the system executes: ADDI R1, R2, #10 where R2 contains the original score, #10 is an immediate bonus value, and R1 stores the updated score Now, analyze and illustrate the datapath modifications required to execute this immediate instruction.		
	(c)	A cache has 8 lines. i) Calculate the cache line for block number 21 using direct mapping. ii) For a 2-way set associative addressing, calculate the set number for block 13.	[2]	
	(d)	What is memory hierarchy? Explain how it improves system performance?	[3]	

3.	(a)	Describe how logical address is translated into physical address.	[2]	CO3
	(b)	What is the purpose of pipeline techniques in computer architecture?	[2]	
	(c)	Due to 4 stage pipelining used a processor executes 6 instructions within 9 units of time. Suppose, one of the students (say Mr. X) can execute the above instructions in which each stage is completed in 3 seconds. Now, can you visualize the systems that are executed by Mr. X? If yes, then demonstrate each stage. Analyze how much (%) execution time is saved owing to using pipelining technique.	[6]	