



Daffodil International University
Faculty of Science & Information Technology
Department of Software Engineering
Final Examination, Spring 2026

Course Code: SE 222; Course Title: Computer Architecture

Batch & Sections: 44 (A to K)

Course Teachers: AS, HKN, HT, AJE

Time: 2:00 Hrs

Marks: 40

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	Compare the effectiveness of direct mapping and associate mapping in terms of hit ratio and searching time.	[Marks-4]	CLO-2 Level-4																				
	b)	Consider a direct mapped cache that has a physical address of 32 bits. Memory block size is 128 bytes and cache memory is 512 KB. Examine the main memory size, number of cache lines in cache memory and cache directory size.	[Marks-6]																					
2.	a)	Illustrate the steps of Booth's algorithm for 2's complement multiplication for the following values: Multiplicand: $(B)_{16}$ Multiplier: $(-2)_{16}$	[Marks-6]	CLO-3 Level-4																				
	b)	Explain branch instructions, skip instructions and procedure instructions with example.	[Marks-6]																					
	c)	Describe the purpose of Overflow bit, Supervisor bit and Interrupt bits in flag register.	[Marks-3]																					
	d)	Transform the following IEEE754 single precision floating point binary number into decimal <table border="1" style="margin: 5px;"><tr><td>1</td><td>01111001</td><td>111101110100000000000000</td></tr><tr><td></td><td></td><td>12345678910</td></tr></table>	1		01111001	111101110100000000000000			12345678910	[Marks-5]														
1	01111001	111101110100000000000000																						
		12345678910																						
3.	a)	<table border="1" style="margin: 5px;"><thead><tr><th colspan="4">Instruction Sets</th></tr></thead><tbody><tr><td>INT Add</td><td>R1</td><td>R2</td><td>R3</td></tr><tr><td>INT Subtract</td><td>R4</td><td>R1</td><td>R6</td></tr><tr><td>INT Division</td><td>R6</td><td>R3</td><td>R5</td></tr><tr><td>INT Multiply</td><td>R7</td><td>R4</td><td>R5</td></tr></tbody></table> Visualize a Five-stage pipelining process for the given instructions where division needs two clock cycles for instruction execution and discuss types of <u>Potential Hazard</u> occurring here?	Instruction Sets				INT Add	R1	R2	R3	INT Subtract	R4	R1	R6	INT Division	R6	R3	R5	INT Multiply	R7	R4	R5	[Marks-5]	CLO-4 Level-31
	Instruction Sets																							
INT Add	R1	R2	R3																					
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INT Division	R6	R3	R5																					
INT Multiply	R7	R4	R5																					
b)	Show the Effective Address (EA) calculation process of Stack and Displacement addressing technique with figure. Investigate the two address machine instruction for the given equation: $Y = A * D - B / C$	[Marks-2+3]																						

IF ID OF E W

0.9658203125

-0.03071594238

32

7, 12, 13
4GB 4×2 6656 bytes
000001
1/6