ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

Daffodil International University

Faculty of Science & Information Technology

Department of Computing and Information System

Class Test-1(Set-A), Summer-2026

Course Code: CIS131,

Course Title: Computer Architecture and Organization

Exam Duration: 45 minutes **Marks: 15**

Imagine a user inputs a command into a computing terminal to execute a basic arithmetic statement: **"5 + 3"**. **(a)** Trace the execution step-by-step across all **five foundational functional units** of a computer: 1. Input Unit 2. Memory Unit 3. Control Unit (CU) 4. Arithmetic Logic Unit (ALU) 5. Output Unit Your trace must be structured chronologically, starting from the exact microsecond the user hits the "Enter" key on the input device up to the final visual presentation of the answer on the display. For each step, explicitly state **what data or control signal is moving** and **which unit is processing it**.	5
(b) Why do the Sign-Magnitude and 1's Complement integer formats present algorithmic inefficiencies for CPU designer teams compared to the modern 2's Complement format? **Highlight at least two distinct structural** disadvantages.	5
(c) Consider a 16-bit register used to store floating-point numbers, where the exponent is represented in excess-32 (biased) form. Determine the 16-bit representation of the decimal number + $(13.5)_{10}$ using an **implicit mantissa** representation.	5

ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

Daffodil International University

Faculty of Science & Information Technology

Department of Computing and Information System

Quiz-2(Makeup), Summer-2026

Course Code: CIS131,

Course Title: Computer Architecture and Organization

Exam Duration: 30 minutes **Marks: 15**

(a) **1+4**

1. What is an Instruction Set Architecture (ISA)? Explain, with a suitable example, how ISA acts as an interface between hardware and software.
2. Translate the expression A = P * (Q + R) - S into instruction sequences for the Stack, Register-memory classes.

(b) **2 + 3**

Register Number	Conventional Name	Usage
$0	$zero	Hard-wired to 0
$1	$at	Reserved for pseudo-instructions
$2 - $3	$v0, $v1	Return values from functions
$4 - $7	$a0 - $a3	Arguments to functions - not preserved by subprograms
$8 - $15	$t0 - $t7	Temporary data, not preserved by subprograms
$16 - $23	$s0 - $s7	Saved registers, preserved by subprograms
$24 - $25	$t8 - $t9	More temporary registers, not preserved by subprograms
$26 - $27	$k0 - $k1	Reserved for kernel. Do not use.
$28	$gp	Global Area Pointer (base of global data segment)
$29	$sp	Stack Pointer
$30	$fp	Frame Pointer
$31	$ra	Return Address
$f0 - $f3	-	Floating point return values
$f4 - $f10	-	Temporary registers, not preserved by subprograms
$f12 - $f14	-	First two arguments to subprograms, not preserved by subprograms
$f16 - $f18	-	More temporary registers, not preserved by subprograms
$f20 - $f31	-	Saved registers, preserved by subprograms

ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

1. Draw and label the MIPS R-type instruction format (fields and bit-widths). Encode i. add $t5, $s3, $s4 (Note: add = 100000; sll = 000000) 2. Draw and label the MIPS I-type instruction format. Encode i. lw $t4, 4($s4) ii. sw $t3, 8($s4) (Note: lw = 100011; sw = 101011)	
(d) 1. Processor P1 (2.4 GHz, Program A): IC = 5,000. Mix & CPI: Branch (20%, CPI=5), Load/Store (40%, CPI=2), ALU (40%, CPI=1.5). Processor P2 (2.6 GHz, Program B): IC = 12,000. Mix & CPI: Branch (25%, CPI=5), Load/Store (50%, CPI=3), ALU (25%, CPI=1.5). a. Calculate the average CPI (CPIavg) for both. b. Calculate the execution time for both. c. Determine which processor is faster and by what speedup factor. 2. A microprocessor's floating-point units are enhanced to run 2.5 times faster, while integer units remain unenhanced. If 40% of a program's instructions are floating-point, calculate the overall system speedup using Amdahl's Law.	**3 + 2**

ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

Daffodil International University

Faculty of Science & Information Technology

Department of Computing and Information System

CT-3(Set-A), Summer-2026

Course Code: CIS131, Section: 20A

Course Title: Computer Architecture and Organization

Exam Duration: 15 minutes **Marks: 15**

1. A CPU has a clock frequency of 2 GHz. What is the duration of one clock cycle?
   a) 0.5 ns b) 1 ns c) 2 ns d) 5 ns
2. Which control signal enables writing data into a CPU register from the ALU or memory?
   a) MemRead b) RegWrite c) MemWrite d) IRWrite
3. A 32-bit virtual address uses a page size of 4 KB. How many bits are used for the Page Offset?
   a) 10 bits b) 12 bits c) 16 bits d) 20 bits
4. In a single-cycle datapath, if the Fetch stage takes 200 ps, Decode takes 100 ps, Execute takes 150 ps, Memory takes 250 ps, and Write-Back takes 100 ps, what is the clock cycle time?
   a) 100 ps b) 150 ps c) 200 ps d) 250 ps
5. A system generates 2,000 memory references. If 1,800 are resolved in L1 Cache, what is the L1 Local Hit Rate?
   a) 85% b) 90% c) 95% d) 96%
6. Out of the 200 references that miss L1 (from Q5), 150 hit in L2. What is the L2 Local Hit Rate?
   a) 65% b) 70% c) 75% d) 80%
7. Which cache write policy updates main memory immediately on every write hit?
   a) Write-Back b) Write-Through c) Write-Allocate d) Write-Around

ourdiu.com | Shared by MD. GOLAM MUSTAKIM NAEEM

8. If a Page Table has 2^{20} entries and each entry (PTE) is 4 bytes, what is the total size of the Page Table?
   a) 1 MB b) 2 MB c) 4 MB d) 8 MB
9. Which register holds the address of the next instruction to be fetched?
   a) MAR b) MDR c) PC d) IR
10. Which register temporarily holds an instruction or data fetched from memory?
    a) MAR b) MDR c) ACC d) PC
11. A Hardwired Control Unit generates control signals using:
    a) Microinstructions stored in ROM
    b) Finite State Machines and logic gates
    c) A microprogram counter
    d) Software interpreters
12. Which unit converts a 16-bit immediate value into a 32-bit operand for the ALU?
    a) Multiplexer b) Sign Extension Unit c) Control Unit d) Register File
13. The Translation Lookaside Buffer (TLB) is primarily used to:
    a) Store recently used page table entries for faster address translation
    b) Store instructions for pipelining
    c) Replace the page table entirely
    d) Handle write-back cache misses
14. A cache has a hit time of 2 cycles and a miss penalty of 100 cycles. If the hit rate is 95%, what is the Average Memory Access Time (AMAT)?
    a) 2.5 cycles b) 5.9 cycles c) 6.9 cycles d) 7.9 cycles
15. If the Valid bit in a Page Table Entry is 0 when the CPU accesses it, what event is triggered?
    a) TLB Hit b) Cache Miss c) Page Fault d) Structural Hazard