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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Midterm Examination, Spring 2025
Course Code: CSE335 Course Title: Computer Architecture and Organization
Level:4 Term:1 Batch:61

Time: 01:30 Hrs **Marks: 25**

Answer ALL Questions [Optional]

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	***a)***	In a world before VLSI, computers were bulky, power-hungry machines with limited processing power. With the advent of VLSI, millions of transistors were integrated onto a single chip, revolutionizing speed, efficiency, and miniaturization. This breakthrough enabled the rise of personal computers, smartphones, and AI-driven technologies. **Discuss** how the integration of multiple transistors into a single IC has influenced the cost, performance, and size of computers.	**[3]**	**CO1**
	b)	Briefly **differentiate** between combinational circuit and sequential circuit.	**[2]**	
2.	***a)***	Suppose, a system stores a **24-bits** binary number in the following memory address **0xA1B2C3FE**. How will the bytes be arranged in both big-endian and little-endian modes? Illustrate with an appropriate diagram.	**[5]**	**CO3**
	b)	**Apply** the 0-operand and 1-operand instruction operation technique in the computer architectures for the following instruction: $$x \leftarrow (a \times b + c / d) \times (e + f)$$ Assume that all data are in registers.	**[5]**	
3.	***a)***	Your memory address is **0x5BF2,** and you want to access the address which is located 5 positions ahead of yours. What will be the new address in hexadecimal format? **Convert** this new address to **16-bits** negative binary representation.	**[5]**	**CO2**
	b)	During a design review, a team presents both schematic diagrams and an HDL description of a new digital system. The review focuses on how accurately these representations capture the intended system behavior and how they facilitate communication among team members. The approach aims to minimize design errors and streamline modifications. **Analyze** how does the integration of schematic diagrams and hardware description languages (HDLs) improve design communication and facilitate error detection in complex systems?	**[5]**	