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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Final Examination, Fall 2025

Course Code: CSE215 **Course Title: Electronic Devices and Circuits**
Level: 2 **Term: 1** **Batch: 67**

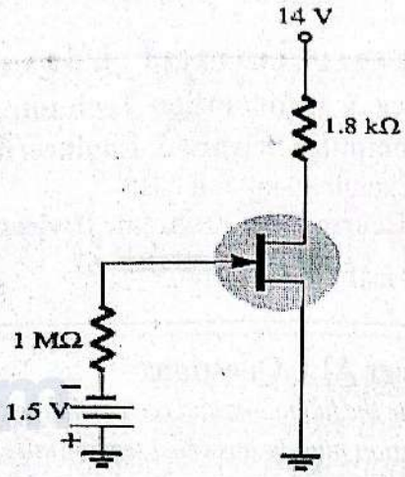
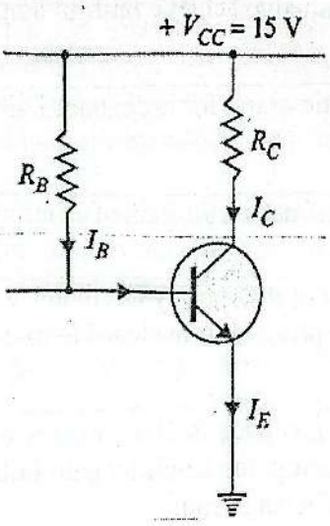
Time: 02:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	*a)*	**Define** the term Decibel gain.	1	CO1
	b)	**Recall** the functions of bypass capacitor in the transistor amplifier.	1	
	c)	**List** the characteristics of an ideal op-amp.	1	
	d)	**Recall** the block diagrams of positive and negative feedback.	1	
	e)	**Name** the conditions must be satisfied to achieve faithful amplification.	1	
2.	*a)*	**Illustrate** the transfer characteristic graph for n-channel D-MOSFET and explain its characteristics.	5	CO2
	b)	**Explain** the impact of negative feedback on the gain of an amplifier with derivation.	5	
	c)	**Demonstrate** the circuit operation of the Hartley Oscillator with the proper circuit diagram and explain how the total phase shift in closed loop is 360 degrees.	5	
3.	*a)*	The gain of an amplifier without feedback is 100 whereas with negative voltage feedback, it falls to 50. If due to ageing, the amplifier gain falls to 80, **Solve** for the percentage reduction in stage gain (i) Without feedback and (ii) With negative feedback.	5	CO3
	b)	An amplifier rated at 40W output is connected to a 10Ω speaker. **Solve** for the value of (i) The input power required for full power output if the power gain is 25 db. (ii) The input voltage for rated output if the amplifier voltage gain is 40 db.	5	

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	c)	For the JFET in Fig. 1, $V_P = 4V$ and $I_{DSS} = 12$ mA. **Solve** for the value of (i) Drain Current, I_D and (ii) Drain-Source voltage, V_{DS}  Fig. 1	5	
	d)	Applying base resistor biasing method for a CE amplifier such that the operating point is $V_{CE} = 8V$ and $I_C = 2$mA with a fixed 15V d.c. supply and a silicon transistor with $\beta = 100$. Here base-emitter voltage $V_{BE} = 0.6V$. **Solve** the biasing circuit for i) The value of R_B and R_C that would be employed in the circuit. ii) Draw d.c. load line.  Fig. 2	5	

Good Luck!!!