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Daffodil International University

Faculty of Science & Information Technology
Department of Software Engineering
Final Examination, Summer 2026
Course Code: SE 222; Course Title: Computer Architecture
Batch & Sections: 45 (A to L)
Course Teachers: MH, KBB, FC, RCDT

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a) ৮	**Explain** the structure and read operation of cache memory with proper diagram.	[Marks-5]	CLO-2 Level-2
	b) ৮	**Distinguish** with reasons between Direct Mapping and Associative Mapping cache strategies.	[Marks-5]	CLO-2 Level-3
2.	a) ৫	**Perform** Booth's algorithm for 2's complement multiplication. A digital signal processor needs to multiply two negative numbers: Multiplicand: -7 and Multiplier: -6 (Using 5-bit representation). Show all iterations step-by-step with proper bit manipulations and verify the final result.	[Marks-5]	CLO-3 Level-3
	b)	**Translate** the following expression into both Zero-address and one-address machine code representations. For a compiler optimization task: $Z = \{(A + B) / (C - D)\} / \{A + B \times (B \times C)\}$.	[Marks-8]	CLO-3 Level-4
	c)	A high-performance scientific calculator used in an engineering simulation system stores numerical values using a custom 24-bit floating-point representation. To reduce storage requirements, each floating-point number is divided into two fields: First 16 bits: Mantissa (represented using 2's complement notation) Last 8 bits: Exponent (represented using 2's complement notation). During a system verification process, two processing units generate the following binary floating-point representations for the same scientific calculation: Data A: 1661161116000000.11111010 Data B: 0111010101011166000000111	[Marks-7]	CLO-3 Level-4

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		As a computer system analyst, you are assigned to investigate how these two floating-point representations are interpreted by the processor and identify the reason for any difference in their stored values. **Calculate** the final decimal value represented by Floating-Point Data A and Floating-Point Data B using the floating-point formula		
3.	a)	**Illustrate** a branch instruction pipeline with timing diagram and explain the impact on pipeline efficiency.	[Marks-5]	CLO-4 Level-3
	b)	An autonomous vehicle control processor uses a 5-stage instruction pipeline—consisting of Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI), and Write Operand (WO)—to optimize execution speed during real-time navigation tasks. Consider a scenario where the processor executes a sequence of 20 instructions, where 5 th instruction is a branch instruction which indicates 17 th instruction. **Draw** the pipeline architecture for an instruction set for the above scenario.	[Marks-5]	CLO-4 Level-4

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