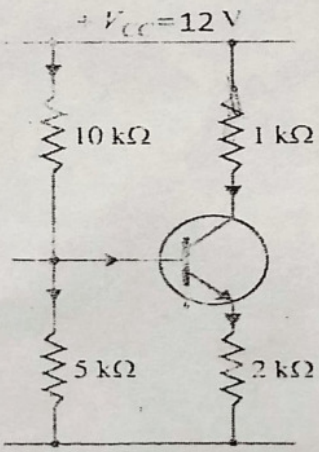
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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science and Engineering
Final Examination, Fall 2024
Course Code: CSE215 Course Title: Electronic Devices and Circuits
Level: 2 Term: 1 Batch: 65

Time: 2:00 Hours **Full Marks: 40**

Answer all the following three questions
[All portions of each question must be answered sequentially]

Q1.	*a.*	**Write** a short note on CMOS.	5x1 =5	CO1
	b.	**Recall** the conditions for the faithful amplification of a transistor.		
	c.	**Show** the virtual ground using a connection diagram of an OP-AMP.		
	d.	**Recall** frequency responses of Multistage Amplifiers.		
	e.	**Define** positive and negative feedback.		
Q2.	*a.*	**Explain** the circuit operation of n-channel D-MOSFET.	3x5 =15	CO2
	b.	**Demonstrate** the practical circuit of the transistor amplifier.		
	c.	**Explain** the operation of Colpitt's and Hartley Oscillators in detail.		
Q3.	*a.*	A JFET has a drain current of 6 mA. If I_{DSS} = 12 mA and V_{GS} (off) = – 6 V, **Solve** for the value of *(i)* V_{GS} and *(ii)* V_P.	4	CO3
	b.	In an amplifier, the output power is 2 watts at 2 kHz and 1 watt at 20 Hz, while the input power is constant at 10 mW. **Solve** for the value of how many decibels the gain at 20 Hz is below that at 2 kHz.	4	
	c.	The following silicon transistor is biased using Voltage Divider Biased Method. **Solve** the biasing circuit for *(i)* the load line and *(ii)* the operating point. 	6	
	d.	The gain of an amplifier without feedback is 100 whereas with negative voltage feedback, it falls to 50. If due to ageing, the amplifier gain falls to 80, **Solve** for the percentage reduction in stage gain *(i)* without feedback and *(ii)* with negative feedback.	6	