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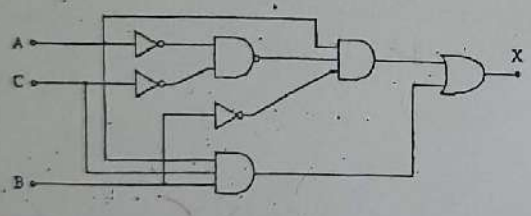
Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Final Examination, Spring 2026
Course Code: SE 213; Course Title: Digital Electronics & Logic design
Sections & Teachers: 45: NIR (A-D), SP (G-J), NJN (E, F, K, L), RRB (M)

Time: 2:00 Hrs. Marks: 40

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	**Compute** the reserve canonical form for following Boolean expression and simplify it using the K-map (consider minterms to construct k map): $F(w,x,y,z) = (w+x+y+z')\,(w+x+y'+z')\,(w+x'+y+z')\,(w'+x+y'+z')$	[Marks-6]	CLO-2 L3
	b)	**Interconvert** the Boolean expression from the following Logic Circuit and simply the expression. 	[Marks-4]	
2.	a)	An Adder within a digital ALU is used to compute the sum of two binary numbers 01110 and 11011. By **constructing** the Adder diagram, perform a bit-wise addition and provide the Sum (S) and Carry-out for every bit position.	[Marks-5]	CLO-3 L3
	b)	**Draw** and configure an Octal to Binary code converter circuit applying the concept of encoder/decoder. Draw the Circuit diagram, truth table and derive the output expressions.	[Marks-5]	
	c)	**Demonstrate** the following Boolean function using an appropriate multiplexer. Show all steps including Implementation table and final design. $F(A, B, C, D) = \Sigma(0, 1, 3, 6, 11, 12, 14)$	[Marks-5]	
3.	a)	Suppose You are operating an SR Latch NAND currently in the SET state (S=1, R=0). Identify the next specific input values for S and R required to transition the circuit into a state to maintain the current output. **Explain** your answer using the SR latch's NAND characteristic logic.	[Marks-3]	CLO-4 L4

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	b)	The SR flip-flop suffers from an invalid state when both inputs are low. **Identify** the specific flip-flop designed to mitigate this issue by using feedback to enable a toggle function instead. Along with the circuit diagram, explain how this new flip-flop modifies the internal logic to ensure a predictable output even when both inputs are active. JK	[Marks- 5]	
	c)	i) In 5-bit shift register: 10011, **illustrate** how many clock pulses are required to change the content of shift register when all 1's (using by XOR gate for last two bit), ii) **Draw** and describe the block diagram of Serial Input Parallel Output (SIPO) Register	[Marks- 3+4]	

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