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CLO-3 Level-5

Daffodil International University

Faculty of Science & Information Technology
Department of Software Engineering
Final Examination, Spring 2026
Course Code: SE 222; Course Title: Computer Architecture
Batch & Sections: 44 (A to K)
Course Teachers: AS, HKN, HT, AJE

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	**Compare** the effectiveness of direct mapping and associate mapping in terms of hit ratio and searching time.	[Marks-4]	CLO-2 *Level-4*
	b)	Consider a direct mapped cache that has a physical address of 32 bits. Memory block size is 128 bytes and cache memory is 512 KB. **Examine** the main memory size, number of cache lines in cache memory and cache directory size.	[Marks-6]	
2.	a)	**Illustrate** the steps of Booth algorithm for 2's complement multiplication for the following values: Multiplicand: $(B)_{16}$ Multiplier: $(-2)_{16}$	[Marks-6]	CLO-3 *Level-4*
	b)	**Explain** branch instructions, skip instructions and procedure instructions with example.	[Marks-6]	
	c)	**Describe** the purpose of Overflow bit, Supervisor bit and Interrupt bits in flag register.	[Marks-3]	
	d)	**Transform** the following IEEE754 single precision floating point binary number into decimal 1 | 01111001 | 11110111010000000000000	[Marks-5]	
3.	a)	**Instruction Sets** INT_Add: R1, R2, R3 INT_Subtract: R4, R1, R6 INT_Division: R6, R3, R5 INT_Multiply: R7, R4, R5 **Visualize** a Five-stage pipelining process for the given instructions where division needs two clock cycles for instruction execution and **discuss** types of Potential Hazard occurring here?	[Marks-5]	CLO-4 *Level-31*
	b)	**Show** the Effective Address (EA) calculation process of Stack and Displacement addressing technique with figure. Investigate the two address machine instruction for the given equation: Y=A*D - B/C	[Marks-2+3]	