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Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Final tern Examination, spring 2025
Course Code: SE 222; Course Title: Computer Architecture
Batch & Sections: 42 (A, B, C, D, E, F, G, H, I, J, K)
Course Teachers: SP, KBB, SC, HK, AAS

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	***a)***	**Explain** briefly what happens during a cache read operation with figure	**[Marks-5]**	**CLO-2** ***Level-2***
	b)	**Explain** with reasons: Why might Set-Associative Mapping be considered a compromise between Direct Mapping and Associative Mapping?	**[Marks-5]**	
2.	***a)***	**Apply** the Booth's algorithm for 2's complement multiplication for the following values: (Using 4 bits) **Multiplicand: -6** **Multiplier: -4**	**[Marks-5]**	**CLO-3** ***Level-3***
	b)	**Investigate** the following expression, representing it as coding for both three-address and one-address representations: $Z = [\{(a * b) + (c * d)\} - (a * b * c)]$	**[Marks-5]**	
	c)	**Calculate** the following floating point binary numbers into decimal. Assuming First 10 bits for the mantissa and Last 6 bits for the exponent, both in 2's complement. i) 0 1 0 1 1 0 0 0 0 0 1 1 1 0 1 1 ii) 1 0 1 1 1 1 0 1 0 0 1 1 1 1 0 0	**[Marks-10]**	
3.	***a)***	**Employ** a two-stage instruction pipelining consisting of fetch and execute stage for discussing the necessity of pipelining along with appropriate figure.	**[Marks-5]**	**CLO-4** ***Level-3***
	b)	**Modify** the pipeline architecture for an instruction set with 20 instructions, following the considerations – 5^{th} instruction is a branch instruction which indicates 17^{th} instruction.	**[Marks-5]**	

CamScanner