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Daffodil International University

Faculty of Science & Information Technology

Department of Software Engineering

Midterm Examination, Fall 2026

Course Code: SE222; Course Title: Computer Architecture

Sections & Teachers: DMH(A-B,F-G), HT(C-E,L), AAA(H-K), AAAS(M-N), FMD(O)

Time: 1 Hour 30 Mins **Marks: 25**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	A program consists of 40% arithmetic instructions at CPI 1, 20% load/store instructions at CPI 4, and 30% branch instructions at CPI 6. All other instructions have a CPI of 8. **Use the information above to answer questions 1(a) - 1(c).**			CLO-1 *Level-2*
	a)	**Compute** the average CPI of the program.	[Marks-1]	
	b)	A processor modification reduces the overall CPI to 3.4 by changing only the load/store instruction CPI. **Estimate** the modified CPI of the load/store instructions.	[Marks-3]	
	c)	Considering that only the branch instructions of the original program can be parallelized, **compute** the minimum number of processors required to achieve an overall speedup of at least 1.25× using Amdahl's Law.	[Marks-3]	
2.	*a)*	A processor chip initially contains 20 million transistors. Assuming the transistor count doubles every three years, **estimate** the time required to reach at least 5 billion transistors using Moore's Law.	[Marks-2]	
	b)	A processor is connected to two I/O devices: Printer and Scanner, with interrupt priorities 2 and 1, respectively, where 1 represents the highest priority. While executing a program, the processor receives the following interrupt requests: • At t = 5s, the Printer generates an interrupt requiring 6s to complete. • At t = 7s, the Scanner generates an interrupt requiring 4s to complete. **Visualize** the complete interrupt execution sequence under nested interrupt handling, specifying the execution order and corresponding start and end times, including any interrupted and resumed operations.	[Marks-3]	
	c)	**Describe** the functions of the major functional units of a computer and visualize the flow of data among these units when a computer operates as a data storage device.	[Marks-3]	

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3.	*a)*	**Trace** the step-by-step execution of the hypothetical processor using the given memory contents, initial CPU register values, and opcode definitions. Illustrate the changes in the Program Counter (PC), Instruction Register (IR), Accumulator (AC), and relevant memory locations after each instruction. Memory: 101 5670; 102 4673; 103 2672; 104 1671; 105 3672; 670 005; 671 006; 672 003; 673 007 Initial CPU Register: AC 010; PC 101; IR **List of opcodes in binary** 0001---Load AC from memory value 0010---Store AC to memory value 0011---Multiply AC by memory value 0100---AC = max(AC, memory value) 0101---Divide AC by memory value	[Marks-5]	CLO-2 *Level-4*
	b)	**Illustrate** the cache memory read operation using a flowchart, clearly distinguishing between cache hit and cache miss.	[Marks-5]	

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