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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Mid Examination, Summer 2025
Course Code: 317 , Course Title: Microprocessor and Microcontroller
Level:L3 Term:T1 Batch: 64

Time: 01:30 Hrs **Marks: 25**

Answer ALL Questions [Optional]

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	*a)*	**Identify** the architectural advancements from the Intel 8086 to the Pentium microprocessor, address the growing demands for computing performance, and discuss what impact did these changes had on software development and system design.	05	CO1
2.	*a)*	While the 8086 is executing a sequence of instructions fetched into its instruction queue, an external hardware interrupt signal (INT 21h) occurs. The CS is 0x2500 and IP is 0x0050 before the interrupt. i.Explain what happens internally in the 8086 when the interrupt is acknowledged, focusing on the BIU and EU interaction. ii.How is the instruction queue affected during interrupt processing? iii.How the flag bits are affected	05	CO2
	b)	**Describe** how the control and status pins of the 8086 microprocessor (such as HOLD, READY, INTR, NMI, and RESET) contribute to managing system operations and interrupts. Write the assembly instructions for the **code segment** to print the string "Hello " on the screen.	05	
3.	*a)*	Consider the 8-bit addition instruction: **ADD** AL, 0x3C where the initial value of the AL register is 0xA7. **Calculate** the values of the Carry Flag (CF), Zero Flag (ZF), Sign Flag (SF), Parity Flag (PF), and Overflow Flag (OF) after the execution of this instruction **DEC AL** **NEG AL** **XCHG AL, BL** **SUB BL, 0x5F** where the initial value of the BL register is 0xA2.	05]	CO3
	b)	For the 8086 microprocessor, **calculate** the effective address in each of the following addressing modes given the register values:BX = 1000H,SI = 0200H,DI = 0300H,BP = 0100H,Displacement = 0050H **i.Register Indirect addressing** **ii.Relative Based Indexed** **iii.Base Indexed**	05	

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		Given the following assembly code snippet:
		CMP AX, BX
		JE EQUAL
		MOV CX, 0
		JMP CONTINUE
		EQUAL:
		MOV CX, 1
		CONTINUE
		What value will be stored in the register CX if AX is equal to BX? What if AX is not equal to BX? **Show** how the JE instruction affects the flow of the program		

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