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Daffodil International University

Faculty of Science & Information Technology

Department of Computer Science & Engineering

Final Semester Examination, Spring 2025

Course Code: CSE335 Course Title: Computer Architecture and Organization

Level: 4 Term: 1 Batch: 61

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions [Optional]

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	A digital control system processes sensor data using a 6-bit binary multiplier. Suppose the system receives **two 6-bit binary** values, **A=101101** and **B=011011**, which represent sensor readings. The system needs to compute their product to determine the control output. **Design** a logic diagram to implement this multiplication for A & B. **Derive** the general equation for **multiplying** two 6-bit binary numbers and apply it to compute the **12-bit binary** product of A and B.	[3+4]	CO2
	b)	A scientist is using a computer to perform complex mathematical calculations, such as simulating weather patterns. The computer's CPU alone is taking too long to complete the calculations. **How coprocessor** helps in this situation?	[3]	
2.	a)	From the below figure **identify** what kind of Hazard it is. **Draw** the necessary diagrams step by step to **eliminate** this particular hazard if there is single port available in every clock cycle.	[1+4]	CO3
	b)	Suppose you have **12 instructions** to process with **no-branch**. Assume that the instruction cycle time is **8 milliseconds**. After identifying the total time required for a pipeline with **7 stages** to execute all the instructions, now find out the **speedup factor**. And **sketch** the graph accordingly.	[3+2]	

Clock Cycle

	1	2	3	4	5	6	7	8	9
Ins-1	FI	DI	CO	FO	EI	WO			
Ins-2		FI	DI	CO	FO	EI	WO		
Ins-3			FI	DI	CO	FO	EI	WO	
Ins-4				FI	DI	CO	FO	EI	WO

Fig 1: Six Stage Pipeline

$\frac{nk}{k+(n-1)}$ 4.66

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3.	a)	Assume you have a **Main Memory** which has a size of **256 Byte** and a **Cache Memory** size of **32 Byte**. **Each line** of cache memory can **hold a block of 32 bits** words, where each **word of size 8 bits**. Now, **sketch** the Cache and Main Memory structure for the above requirements, then **show the Associative Mapping** from Cache to Main Memory with example of **Address Structure** using 000000111 address.	[3+4]	CO4
	b)	**Analyze** which mapping within 3 types, will be effective for the above scenario with the required parameters: **Data Loss, Speed, Time**.	[3]	
4.	a)	*A system administrator at a data center observed unusual memory access patterns processes were accessing segments they typically shouldn't and triggering unexpected page faults, suggesting a potential security breach. Recalling that the Memory Management Unit (MMU) is essential for translating virtual addresses to physical addresses and enforcing memory protection, the administrator initiated an investigation into the MMU's role in system security.* **Analyze** the role of the Memory Management Unit (MMU) in translating virtual addresses to physical addresses to ensure that processes access only their allocated memory. **Evaluate** the effectiveness of memory access time **with a mathematical example** if page hit and page fault occurs.	[3+4]	CO4
	b)	**Discuss** with the help of a diagram that how the demand paging affects overall system performance.	[3]	

0 − 1 = 1 --1