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Daffodil International University
Department of Software Engineering
Faculty of Science & Information Technology
Midterm Examination; Fall 2024
Course Code: SE222 ; Course Title: Computer Architecture
Sections & Teachers: KBB, SUP, SS, MS, SR, SSD
Time: 1 Hour 30 Mins **Marks: 25**

Answer ALL Questions
[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1. a) **Describe** the program flow of control without and with the use of interrupts when performing an I/O operation. [Marks-3]

b) A 2 GHz processor was used to execute on a program with the following instruction mix and clock cycle counts:

Instruction Type	Frequency	CPI
Integer ALU operation	10%	1
Floating point Operation	40%	17
Loads & Stores	30%	5
Branches	20%	3

[Marks-3]

Compute the effective CPI, MIPS rate from the table to execute program delivery. CLO-1 *Level-2*

c) **Convert** the Hypothetical Processor Instructions from the generated figure. [Marks-5]

Memory

101	3606
102	6607
103	7608
104	4609
606	0007
607	0005
608	0003
609	0008

Here,

0011 → load AC from memory 3
0100 → store AC to memory 4
0110 → Subtract to AC from memory 6
0111 → Multiply to AC from memory 7

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	d)	Assume that your processor is working with 9 I/O devices: a keyboard, a portable disk, a pen drive, a headphone, a mouse, an audio system, a DVD-ROM, a printer, and a scanner. The priorities of these devices are 1, 2, 3, 4, 5, 6, 7, 8, and 9, respectively. **Describe** the multiple interrupt handling with proper diagrams using the following cases: Cases: 1. The processor first receives a signal from the pen drive at time t = 13 units. 2. It then receives a signal from the headphone at time t = 14 units. 3. After that, the processor receives a third signal from the mouse at time t = 15 units. 4. The processor next receives a signal from the portable disk at time t = 16 units. 5. Then, it receives a signal from the audio system at time t = 17 units. 6. The processor receives the sixth signal from the keyboard at time t = 19 units. 7. At time t = 21 units, the processor receives a signal from the DVD-ROM. 8. Afterward, the processor receives a signal from the printer at time t = 22 units. 9. Finally, the processor receives a signal from the scanner at time t = 23 units. → NB: Each task is continuous and can only be completed after handling the interrupts in accordance with their respective priorities.	**[Marks-4]**	
2.	*a)*	**Characterize** the principles of cache memory organization along with a proper diagram.	**[Marks-5]**	**CLO-2** *Level-2*
	b)	**Differentiate** the logical and physical cache diagram with explanations.	**[Marks-5]**	