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Daffodil International University

Faculty of Science & Information Technology

Department of Computer Science and Engineering

Final Semester Examination, Spring-2024

Course Code: CSE335/CSE411 Course Title: Computer Architecture and Organization

Level & Term: L3-T1, L4-T1, L4-T2

Exam Duration: 2.0 Hours **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.		Imagine you are a computer architect, your task is to make an efficient CPU design by utilizing Arithmetic Logic Unit (ALU). And your goal is to achieve superior performance through parallel processing and optimizing hardware for arithmetic and trigonometric operations.		CO2
	a)	Why ALU is important for computer architecture and organization for modern computers. Justify your logic with proper requirements.	[5]	
	b)	Show the efficient hardware implementation strategies you would employ for performing arithmetic operations and trigonometric functions within your CPU design.	[5]	
2.	a)	Consider a pipeline with 6 stages, executing 50 instructions without branching. If the total time required for this pipeline to execute these instructions is (T), find the speedup factor for this scenario. Sketch the effect of a conditional branch in the context of pipelining operation with brief discussion?	[5]	CO3

	b)	Which type of hazard is present in the following scenarios? Provide your logical reasoning with required diagram to solve the following scenarios.
		
		i. SUB R1, R2, R3
		ADD R4, R1, R5
		ii. ADD R1, R2, R3
		ADD R1, R4, R5
			[5]	

3.		Suppose, the cache can hold 64 Kbyte. Data can be transferred between main memory and the cache in block of 4 bytes each. If cache is 16k then 2^{14} lines of 4 bytes each. Main memory consists of 16Mbytes where 24 bit address directly addressable. That means 2^{24} = 16M. So, 4M blocks of 4 bytes each. Additionally, it has a direct-mapped cache.		CO4

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	a)	Discuss the cache mapping with address format and required mapping diagram for this system, considering the specifications mentioned above. Also Propose a transition plan to enhance the cache structure by changing it to a 4-way set-associative cache. How would the address format change with this new cache configuration?	[5]	
	b)	Define the memory hierarchy with the performance factors. Sketch the Cache Read Operation flowchart.	[5]	
4.		You are a computer architect working on designing a new system for a company that specializes in data-intensive applications, such as large-scale database management and analytics. The system is intended to handle massive amounts of data while providing efficient memory management to ensure optimal performance. As part of your design, you've proposed implementing a virtual memory system.		CO4
	a)	Sketch the address translation mapping technique of virtual memory with proper figures to identify the necessary parameters of virtual memory.	[5]	
	b)	Show the sharing process of virtual memory with proper diagrams. And list the advantage and disadvantages of virtual memory for large data scale.	[5]	

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