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Daffodil International University

Department of Electrical and Electronic Engineering

Faculty of Engineering

Midterm Examination, Spring-2026

Course Code: 0714-323 | Course Title: Digital Electronics
Section: A, B, C | Level-Term: L3-T1 | Teacher's Initial: DAS, BS
Full Marks: 25 | Exam Date: February 28, 2026 | Time: 1.5 Hours

[Notes: Answer all the questions. The number on the rightmost side of the question indicates the marks.]

Q1.	(a) **Perform** the following subtraction operation using both $r's$ and $(r-1)'s$ complement: $7B4C)_{16} - A9F)_{16}$	CO1 (C2)	3+3+3
	(b) **Simplify** the following Boolean function to a minimum number of literals using the laws of Boolean algebra: $F(A,B,C,D) = A + (B + C'D)' + A'BC + A(A' + D) + 0$	CO1 (C3)	
	(c) **Implement** the half-subtractor circuit using: i) NAND gates, ii) NOR gates	CO3 (C3)	
Q2.	(a) **Express** the Boolean function, $F(A,B,C) = C'$ in sum of minterms and product of maxterms.	CO1 (C3)	4+4
	(b) Using K-map **find** the simplest form in SOP and POS for the following **Boolean function:** $F(w,x,y,z) = \sum(0,2,3,6,7)$ **with the don't care conditions given by:** $d(w,x,y,z) = \sum(8,10,11,15)$	CO1 (C3)	
Q3.	(a) **Define** the following performance parameters of digital ICs: i) Noise Margin, ii) Propagation Delay	CO2 (C1)	2+3
	(b) **Draw** neat and properly labeled circuit diagrams of the following: i) CMOS NOR, NAND gates, ii) Modified DTL NAND gate	CO2 (C2)	
Q4.	Suppose you are asked to design an 84−2−1 to 2421 code converter circuit. Are there any don't-care states in this design? If so, **identify** them.	CO3 (C3)	3