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Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science and Engineering Mid Semester Examination, Fall-2025
Course Code: CSE335 Batch: 62
Course Title: Computer Organization & Architecture
Level:2 Term:1

Exam Duration: 1.5 Hours **Marks: 25**

Answer ALL Questions [Optional]

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	*a)*	Modern computer organization uses three design levels: processor level, register level, and gate level. Explain how a simple ADD instruction is represented differently at each of these three levels, providing specific examples of components and operations at each level.	[3]	CO1
	b)	A RISC processor uses fixed-length 32-bit instructions, while a CISC processor uses variable-length instructions (1 to 6 bytes). Evaluate the advantages and disadvantages of each approach in terms of: (i) Memory usage, (ii) Instruction decoding complexity, (iii) Instruction prefetching efficiency. Provide a specific example for each point.	[2]	
	c)	Distinguish Between analysis & synthesis in the context of computer system design. Illustrate your answer with a suitable example from digital logic design.	[2]	
2.	*a)*	The binary number $(11010110)_2$ is stored in memory. Determine what this represents in: (i) Unsigned decimal, (ii) Signed decimal using 2's complement, (iii) Hexadecimal, (iv) Octal.	[5]	CO2
	b)	Modern CPUs employ various addressing modes. Given the following: Register R1 contains 0x3000, Memory location 0x3000 contains 0x4050, Memory location 0x4050 contains 0x1234. Determine what data is accessed using: (i) Register addressing: R1, (ii) Register indirect: M[R1], (iii) Immediate: #0x3000, (iv) Direct: M[0x3000], (v) Indirect: M[M[0x3000]].	[4]	
	c)	An instruction ADD R1, R2, R3 is to be executed where R1=0x0A, R2=0x15, R3=0x20. Apply this instruction using: (i) Three-operand format and (ii) Two-operand format,. Show register contents after execution in each case.		

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3.	*a)*	The system bus connects CPU, memory, and I/O devices using three types of buses: control bus, data bus, and address bus. Analyze the role of each bus type during a memory read operation, explaining the sequence of signals and data flow. Construct a diagram showing the interaction between these buses.	[5]	CO3
	b)	A 32-bit system stores the hexadecimal value 0x1A2B3C4D starting at address 0x1000 in little-endian format. Show the exact byte-by-byte memory layout from address 0x1000 to 0x1003. Then explain and show what would change if the same data were stored in big-endian format.	[4]	