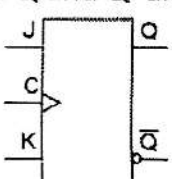
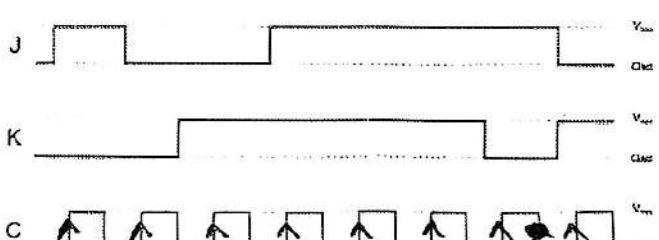
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Classtest 3

CSE223: Digital Logic Design

Time: 50 minutes Marks: 15

1.	From the given F (A, B, C, D) =Σ (1,3,4,6,8,10,11,14), build a 4*1 multiplexer where selection lines are: A, D.	5
2.	Explain how the JK flip-flop resolves the indeterminate ('invalid') state problem of the SR flip-flop. Provide a clear comparison between the two flip-flops and illustrate your explanation with truth tables and behavior at the clock edge.	5
3.	From the given timing diagrams, find Q and Q' diagram.  	5