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Makeup Test (Quiz 01)

Student ID: _____ Student Name: _____

Course Code: CIS131 **Course Title: Computer Architecture and Organization**
Semester: Summer 2026 **Section: _____** **Date: 06.08.2026**
Exam Duration: **15 mins** Marks: **15**

1. **Which register holds the address of the next instruction to be executed?**
   ☐ ACC ☐ IR
   ☐ PC ☐ MDR

2. **IEEE 754 double precision floating point uses how many bits?**
   ☐ 32 bits ☐ 16 bits ☐ 64 bits ☐ 128 bits

3. **Which cycle does the Control Unit manage?**
   ☐ Read-Write-Store ☐ Input-Process-Output
   ☐ Fetch-Decode-Execute ☐ Compile-Run-Debug

4. **Which register stores intermediate results during computation?**
   ☐ IR ☐ MDR ☐ PC ☐ ACC

5. **How many bits does ASCII use?**
   ☐ 4 ☐ 7 ☐ 128 ☐ 16

6. **Which generation of computers introduced Microprocessors?**
   ☐ Second ☐ Third ☐ Fourth ☐ Fifth

7. **In Packed BCD format, how many decimal digits are stored per byte?**
   ☐ 1 ☐ 1 ☐ 4 ☐ 8

8. **In BCD, each decimal digit is encoded into:**
   ☐ 4 bits ☐ 8 bits ☐ 2 bits ☐ 16 bits

9. **For the value 450 (0x000001C2), what is the first byte stored in Little-endian format?**
   ☐ 00 ☐ 01 ☐ C2 ☐ 1C

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10. In MIPS I-type format, how many bits are used for the constant/address field?

☐ 6 bits ☐ 5 bits ☐ 16 bits ☐ 26 bits

11. If the exponent in a floating-point representation is stored in excess-256 form, how many bits (k) are required for the exponent field?

☐ 8 ☐ 9 ☐ 7 ☐ 10

12. BCD works directly on which radix?

☐ Radix 2 ☐ Radix 8 ☐ Radix 10 ☐ Radix 16

13. "Add r1, 100(r2)" represents which addressing mode?

☐ Indexed addressing ☐ Memory indirect addressing

☐ Displacement addressing ☐ Auto-increment addressing

14. Consider the fixed notation <6,2> and find the 2's complement fixed-point representation of the decimal number -6.25.

☐ 1001.11 ☐ 0110.01 ☐ 10.0111 ☐ 01.1001

15. Which instruction encoding is used by ARM and MIPS?

☐ Variable length ☐ Fixed length (32-bit)

☐ Variable length (1–18 bytes) ☐ 64-bit fixed length