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Q3.	(a) **Design** a counter with JK flip-flops which count binary sequence of 0, 1, 3, 2, 6, 4, 5, 7 and repeat.	CO3 C3	7+3
	(b) **Draw** a 4-bit register using D flip-flops with parallel loading ability.		
Q4.	The state diagram of a clocked sequential circuit is given in Figure 2. **Design** the circuit using T flip-flops and after detailed analysis draw the complete logic diagram of the circuit.	CO3 C4	10

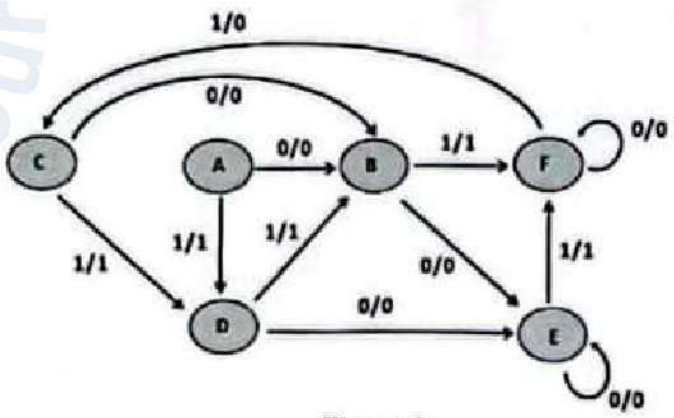


Figure 2

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Daffodil International University

Department of Electrical and Electronic Engineering
Faculty of Engineering
Final Examination, Spring – 2026

Course Code: 0714-323	Course Title: Digital Electronics	
Section: A, B, C	Level-Term: L3-T1	Teacher's Initial: DAS, BS
Full Marks: 40	Exam Date: April 25, 2026	Time: 2 Hours

[Notes: The number on the rightmost side of the question indicates the marks]
Answer all Questions

Q1. (a) **Implement** the following Boolean expressions using Decoder and external gates. CO3 C3 **6+4**

$F_1(x, y, z) = x'y'z' + xz$
$F_2(x, y, z) = xy'z' + x'y$
$F_3(x, y, z) = x'y'z + xy$

(b) An 8 × 1 multiplexer has inputs x, y, and z connected to the selection inputs s_2, s_1, and s_0 respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0; I_3 = I_5 = 1; I_0 = I_4 = A; I_6 = A'$ **Determine** the Boolean function implemented by the multiplexer. C4

Q2. (a) **Design** a combinational circuit using a PLA to convert BCD input into its corresponding Excess-3 code. CO3 C3 **6+4**

(b) **Write down** the differences between combinational and sequential logic. A JK flip-flop is triggered by negative clock transitions. **Draw** the output waveform, Q for the flip-flop for the given clock and input waveforms as shown in Figure 1. Assume that the flip-flop is initially in the Reset state (Q = 0). CO3 C3

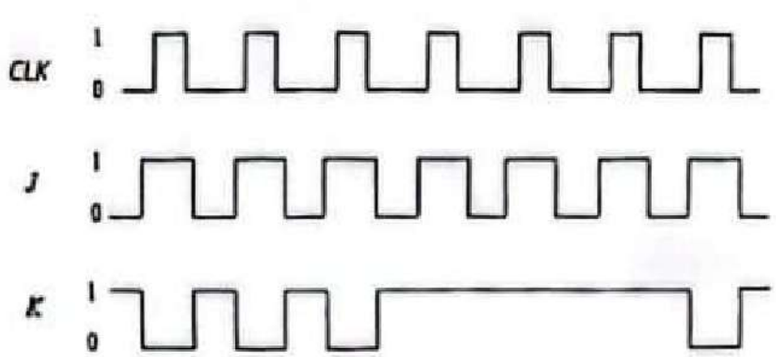


Figure 1