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Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Final Examination, Fall 2025
Course Code: SE 213, Course Title: Digital Electronics & Logic Design
Batch:44; Sections: A, B, C, D, E, F, G, H, I, J, K, L
Teachers: SP, HI, NIR, MTE, MTM

Time: 2:00 Hrs. **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	**Apply** k-map simplification technique to simplify the expressions and construct the logic diagrams of the simplified output following below: $F(A, B, C, D) = \sum (0, 1, 5, 7, 9, 10, 11, 12, 13, 14, 15)$	[Marks-5]	CLO-2 L3
	b)	**Change** the following function into its POS form: $F = XZ' + Y'Z'$ and draw the corresponding logic circuit representation.	[Marks-5]	
2.	a)	**Construct** and configure an Octal to Binary Encoder circuit for appropriate binary input. Draw the Circuit diagram, truth table and derive the output expressions.	[Marks-5]	CLO-3 L3
	b)	**Demonstrate** the following Boolean function using an 8:1 multiplexer. $F(A, B, C, D) = \Sigma (0,2, 5, 7, 9, 10, 11, 15)$	[Marks-5]	
	c)	**Derive** the following function applying the concept of decoder: F(w,x,y,z)= w'x'y'z + w'x'yz + w'xyz +wx'yz' +wxy'z' + wxyz'	[Marks-5]	
3.	a)	i) **Show** the difference between sequential circuit and combinational circuit. ii) **Construct** S-R Latch along with circuit diagram and truth table.	[Marks-2 +3]	CLO-4 L3
	b)	Explain the T Flip-Flop, and **demonstrate** operation along with truth table, characteristic table and an excitation table.	[Marks-4]	
	c)	**Illustrate** the working principle of Serial Input Serial Output (SISO) shift register along with block diagram.	[Marks-6]	